Fig.1.

Fig.2.

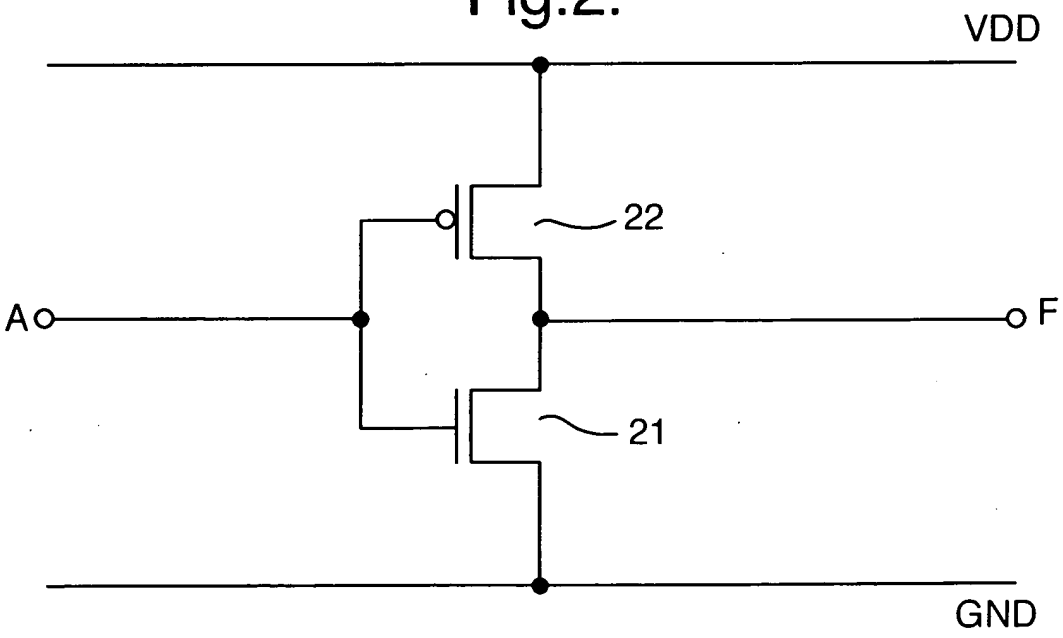


Fig.3.

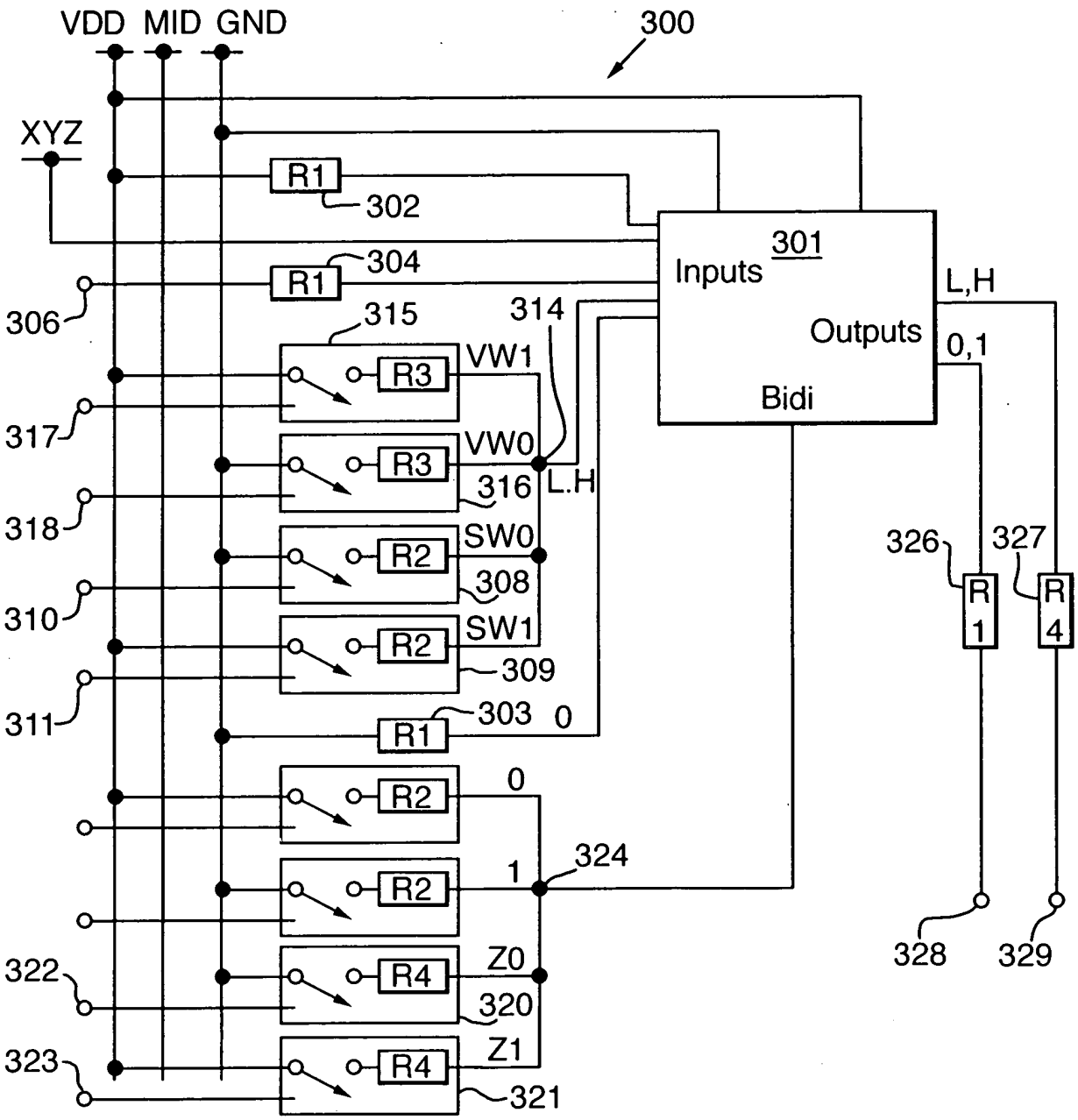

VDD MID GND
300
XYZ
R1
302
R1
304
306
315
314
R3
VW1
317
R3
VW0
316
L.H
318
R2
SW0
308
310
R2
SW1
309
311
R1
303
0
R2
0
R2
1
324
322
R4
Z0
320
323
R4
Z1
321
301
Inputs
Outputs
Bidi
L,H
0,1
326
327
R 1
R 4
328
329

Fig.4.

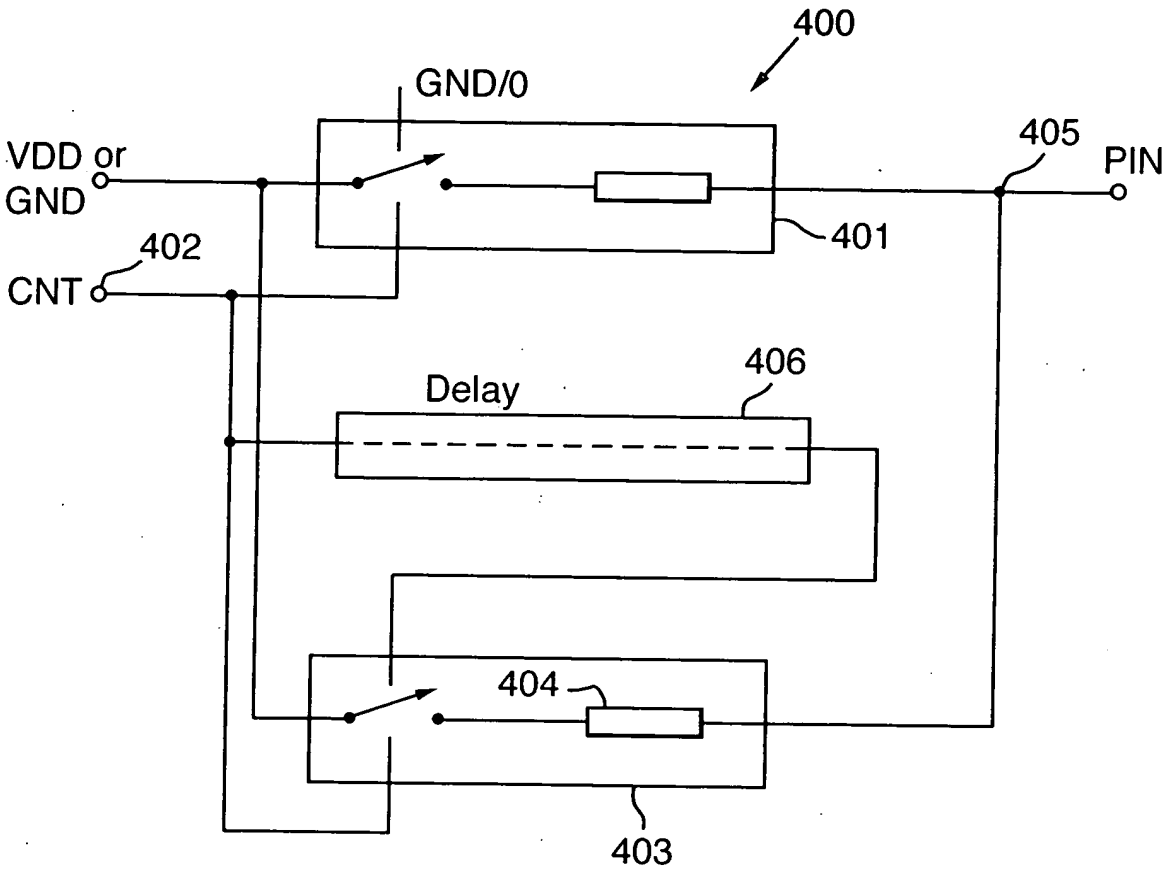


Fig.5.

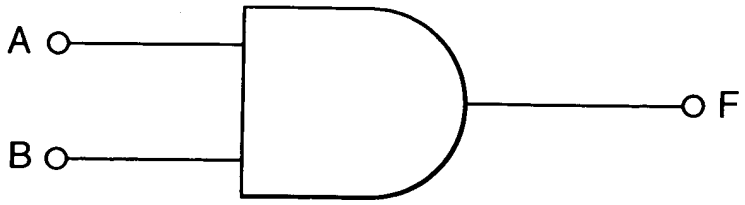
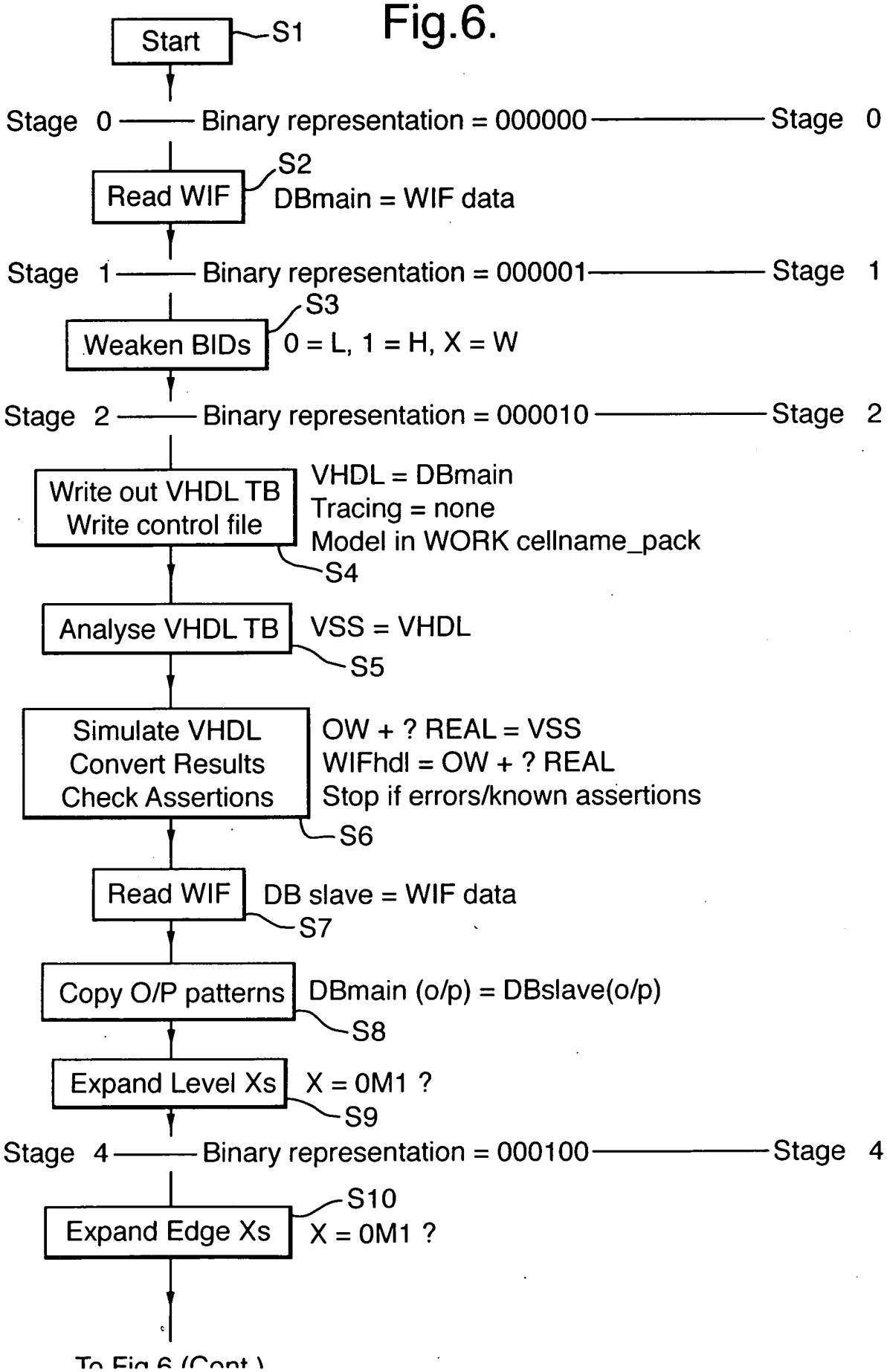
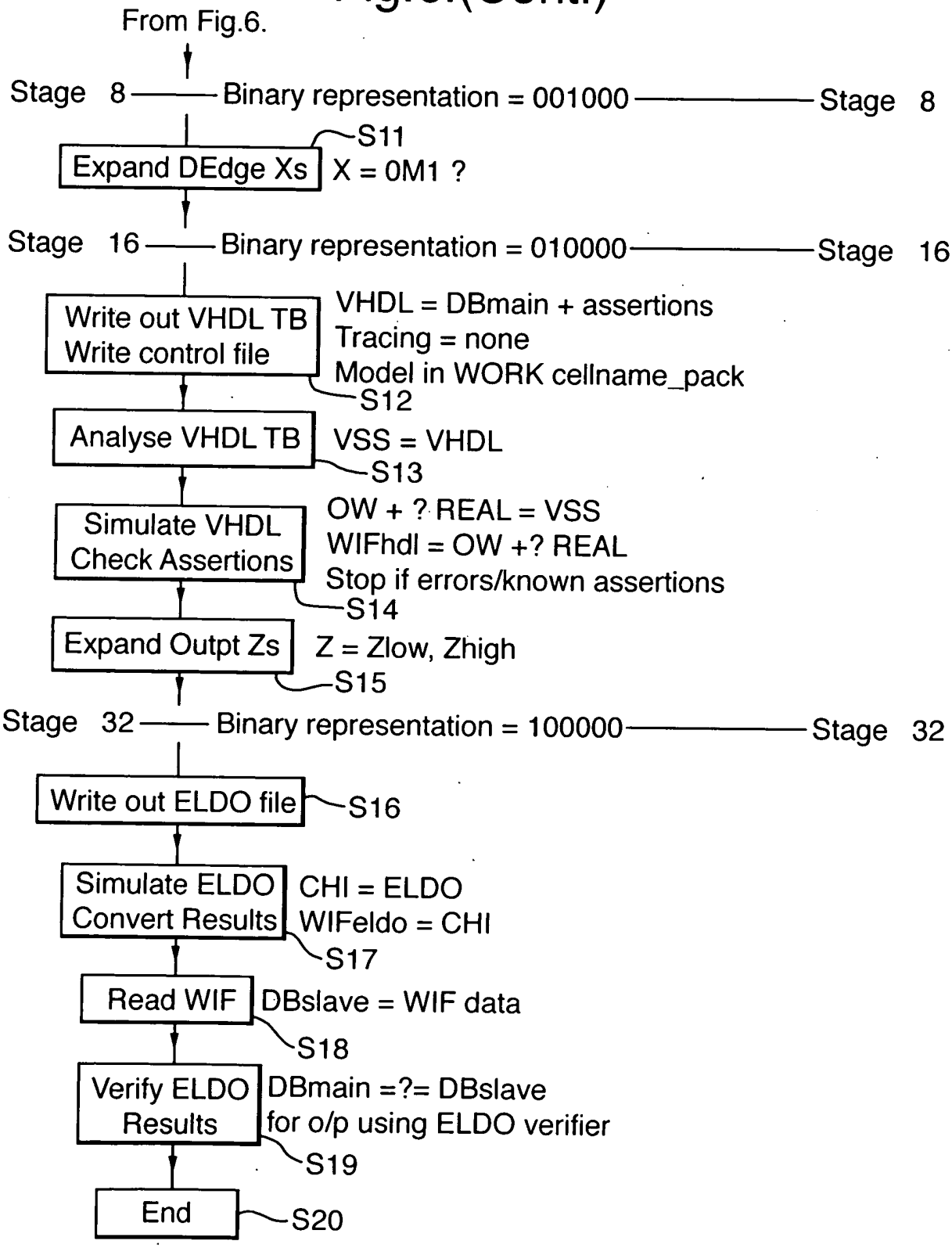


Fig.6.



To Fig.6 (Cont.)

Fig.6.(Cont.)


From Fig.6.
Stage 8
Binary representation = 001000
Stage 8
S11
Expand DEdge Xs
X = 0M1 ?
Stage 16
Binary representation = 010000
Stage 16
Write out VHDL TB
Write control file
VHDL = DBmain + assertions
Tracing = none
Model in WORK cellname_pack
S12
Analyse VHDL TB
VSS = VHDL
S13
Simulate VHDL
Check Assertions
OW + ? REAL = VSS
WIFhdl = OW +? REAL
Stop if errors/known assertions
S14
Expand Outpt Zs
Z = Zlow, Zhigh
S15
Stage 32
Binary representation = 100000
Stage 32
Write out ELDO file
S16
Simulate ELDO
Convert Results
CHI = ELDO
WIFeldo = CHI
S17
Read WIF
DBslave = WIF data
S18
Verify ELDO
Results
DBmain =?= DBslave
for o/p using ELDO verifier
S19
End
S20